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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,930	03/12/2004	Minoru Oka	OMRNP081	6825

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EXAMINER	
BARNES, CRYSTAL J	

ART UNIT	PAPER NUMBER
2121	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,930	OKA ET AL.	
	Examiner	Art Unit	
	Crystal J. Barnes	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a second Non-Final Office Action in response to the Amendment received on 31 August 2005. Claims 1-9 remain pending in this application.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The replacement drawings and amendments to the specification were received on 31 August 2005. These corrections are acceptable.

Response to Arguments

4. Applicant's arguments, see Remarks page 7, filed 31 August 2005, with respect to the rejection of claims 1-9 under 35 USC 102(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

However, upon further consideration, a new ground(s) of rejection is made in view of USPN 5,600,807 to Itoh et al.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by USPN 5,600,807 to Itoh et al.

As per claim 1, the Itoh et al reference discloses a control system comprising: a programmable controller (see column 2 lines 40-42, "programmable controller") including a CPU unit ("CPU module 15") that carries out cyclic operations (see column 2 lines 44-56, "sequence processor") of I/O refresh ("PI/O bus 14"), user program execution ("program executing microcomputer 3") and peripheral service processes ("PI/O bus controller 7"); and a programming tool ("program controlling microcomputer 1") that edits said user program ("user

programs"); wherein said programming tool ("program controlling microcomputer 1") has the functions of uploading (see column 3 lines 52-56, "read from") and downloading (see column 4 lines 14-18, "store into") said user program ("user programs") from and to said programmable controller ("programmable controller"); and wherein said CPU unit ("CPU module 15") includes two memories (see column 2 line 47, "two user program memories 5a, 5b") for storing said user program ("user programs") and has the functions of: selecting (see column 2 lines 57-60, "memory selecting register 6") one of said two memories ("user program memories 5a, 5b"), when said programming tool ("program controlling microcomputer 1") carries out an editing process (see column 4 lines 4-10, "modify") on said user program ("user programs") while said cyclic operations (see column 3 lines 52-60, "processing an instruction") are being carried out, and the user program ("user programs") stored in said selected memory ("user program memories 5a, 5b") to be the object of execution ("program executing microcomputer 3"); uploading ("read from") said programming tool ("program controlling microcomputer 1") and thereby outputting the user program ("user programs") stored in selected one of said two memories ("user program memories 5a, 5b") to said programming tool ("program controlling microcomputer 1") while said peripheral service processes ("processing an

instruction") are being carried out; storing (see column 4 lines 16-18, "store"), while said peripheral service processes ("processing an instruction") are being carried out, a user program ("user programs") downloaded from ("store into") said programming tool ("program controlling microcomputer 1") in the other of said memories ("user program memories 5a, 5b") not storing a user program ("user programs") being executed ("program executing microcomputer 3"); switching (see column 4 lines 42-44, "interruption") the user program ("user programs") stored in the other memory ("user program memories 5a, 5b"), after the downloaded user program ("user programs") has completely been stored in the other memory ("user program memories 5a, 5b"), to become executed ("program executing microcomputer 3"); and copying and storing (see column 4 lines 16-25, "store, copied") the user program ("user programs") stored in the other memory ("user program memories 5a, 5b") to and in the selected memory ("user program memories 5a, 5b").

As per claim 2, the Itoh et al. reference discloses said CPU unit further has the function of further switching ("interruption") the object of execution (see column 4 lines 30-32, "new execution") from the user program ("user programs") stored in the other memory ("user program memories 5a, 5b") to the user program

("user programs") stored in the selected memory ("user program memories 5a, 5b") when said programming tool ("program controlling microcomputer 1") edits ("modify") the user program ("user programs") stored in the other memory ("user program memories 5a, 5b") while said cyclic operations ("processing an instruction") are being carried out.

As per claim 3, the Itoh et al. reference discloses a CPU unit adapted to upload and download a user program between a programming tool and to carry out cyclic operations of I/O refresh, user program execution and peripheral service processes; said CPU unit (see column 2 lines 44-51, "CPU module 15") comprising two memories ("two user program memories 5a, 5b") for storing said user program ("user programs") and having the functions of: selecting (see column 2 lines 57-60, "memory selecting register 6") one of said two memories ("user program memories 5a, 5b"), when said programming tool ("program controlling microcomputer 1") carries out an editing process (see column 4 lines 4-10, "modify") on said user program ("user programs") while said cyclic operations (see column 3 lines 52-60, "processing an instruction") are being carried out, and the user program ("user programs") stored in said selected memory ("user program memories 5a, 5b") to be the object of execution ("program executing microcomputer 3"); uploading ("read

from") said programming tool ("program controlling microcomputer 1") and thereby outputting the user program ("user programs") stored in selected one of said two memories ("user program memories 5a, 5b") to said programming tool ("program controlling microcomputer 1") while said peripheral service processes ("processing an instruction") are being carried out; storing (see column 4 lines 16-18, "store"), while said peripheral service processes ("processing an instruction") are being carried out, a user program ("user programs") downloaded from ("store into") said programming tool ("program controlling microcomputer 1") in the other of said memories ("user program memories 5a, 5b") not storing a user program ("user programs") being executed ("program executing microcomputer 3"); switching (see column 4 lines 42-44, "interruption") the user program ("user programs") stored in the other memory ("user program memories 5a, 5b"), after the downloaded user program ("user programs") has completely been stored in the other memory ("user program memories 5a, 5b"), to become executed ("program executing microcomputer 3"); and copying and storing (see column 4 lines 16-25, "store, copied") the user program ("user programs") stored in the other memory ("user program memories 5a, 5b") to and in the selected memory ("user program memories 5a, 5b").

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,600,807 to Itoh et al. in view of Wilburn.

As per claim 4, the Itoh et al. reference discloses a method of editing a user program of a programmable controller by using a programming tool, said programmable controller being connected to a CPU unit having two memories for storing a user program and adapted to carry out cyclic operations of I/O refresh, user program execution and peripheral service processes; said method comprising the steps of: preliminarily storing said user program in said two memories with same contents; selecting (see column 2 lines 57-60, "memory selecting register 6") the user program ("user program") stored in a selected one of said two memories (see column 2 line 47, "two user program memories 5a, 5b") as the object of execution (see column 2 lines 44-45, "program executing microcomputer 3") before

said user program ("user program") is edited (see column 4 line 5, "modify") with said programming tool (see column 4 lines 14-22, "program controlling microcomputer 1") and continuing said cyclic operations (see column 3 lines 55-56, "processing an instruction") by the CPU unit (see column 2 lines 41-42, "CPU module 15"); uploading a user program (see column 3 lines 52-56, "read out the user program") stored in either of said two memories ("user program memories 5a, 5b") with said programming tool ("program controlling microcomputer 1") while said CPU unit ("CPU module 15") is in operation, and editing ("modify") said uploaded user program ("read out the user program") with said programming tool ("program controlling microcomputer 1"); downloading the edited user program (see column 4 lines 16-18, "store the updated user program"), after said step of editing ("modify") is completed and while said CPU unit ("CPU module 15") is in operation, to the other of said two memories ("user program memories 5a, 5b") and storing said downloaded user program "store the updated user program") with said programming tool ("program controlling microcomputer 1"); causing said CPU unit ("CPU module 15"), after said step of downloading ("store") is completed, to switch ("memory selecting register 6") the object of execution (see column 4 lines 30-32, "new execution") from the user program ("user program") in said selected memory ("user

program memories 5a, 5b") to the user program ("user program") in the other memory ("user program memories 5a, 5b") and to execute ("execution") the edited user program ("updated user program") wherein said CPU unit ("CPU module 15") is arranged to execute ("execution") the edited user program ("updated user program"); and causing said CPU unit to store the edited user program of the other memory to the selected memory thereby causing said two memories to store user programs with same content.

The Itoh et al. reference does not expressly disclose preliminarily storing said user program in said two memories with same contents and causing said CPU unit to store the edited user program of the other memory to the selected memory thereby causing said two memories to store user programs with same content.

The Wilburn reference discloses

(see column 3 lines 41-45, "... allow modification or editing of a program memory ... continuously and interactively controlled by a microprocessor 31 with which the program memory is associated.")

(see column 4 lines 6-12, "... a first program memory 41 ... a second program memory 43 which is essentially similar to the first program memory 41.")

(see column 4 lines 46-48, "The editor 67 ... implement changes in a program memory ...")

(see column 5 lines 39-43, "The editing or patching process ... introduce any desired changes into the algorithms in the program memory being edited without affecting the executing program memory.")

(see column 6 lines 10-14, "... the executing program memory is replaced by with the edited program memory without interrupting operative control of the microprocessor 31")

(see column 6 lines 24-34, "... the algorithms in the first and second program memories will, at some initial time , be identical")

(see column 6 lines 45-60, "... the former executing memory will be placed in the edit mode and the edited memory will become the executing memory ... such interchange of the memories can be accomplished without interruption of the interactive control provided by the microprocessor 31 ... the same editorial changes can be introduced into the formerly executing program.")

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the user program memories taught by the

Itoh et al. reference to include identical user programs initially and finally as taught by the Wilburn reference.

One of ordinary skill in the art would have been motivated to modify the user program memories to include identical user programs in the user program memories initially and finally to provide a programmable controller which is capable of editing, verifying, and replacing a user program easily and quickly.

As per claim 5, the Itoh et al. reference discloses said steps of uploading and downloading ("read out from, stored into") are from and to the memory ("user program memory 5a, 5b") storing the user program ("user program") being executed (see column 3 lines 52-60, "executing") by said CPU unit ("CPU module 15") in said cyclic operations ("sequence processor").

As per claim 6, the Itoh et al. reference discloses said steps of uploading and downloading ("read out from, stored into") are executed while said CPU unit ("CPU module 15") is executing (see column 3 lines 52-60, "executing") said peripheral service processes (see column 2 line 46, "PI/O bus controller 7").

As per claim 7, the Itoh et al. reference discloses said CPU unit ("CPU module 15"), when the user program ("user program") is edited next by said programming tool ("program controlling microcomputer 1"), switches ("memory

selecting register 6") the object of execution ("new execution") from the other memory ("user program memories 5a, 5b") to the selected memory ("user program memories 5a, 5b") and maintains the object of execution ("new execution") thus switched ("memory selecting register 6") until the downloading of the edited user program is completed (see column 4 lines 42-48, "accepts interruption").

As per claim 8, the Itoh et al. reference discloses said CPU unit ("CPU module 15"), when the user program ("user program") is edited next by said programming tool ("program controlling microcomputer 1"), keeps the object of execution (see column 4 lines 30-32, "executed") unchanged from the other memory ("user program memories 5a, 5b") and continues to carry out said cyclic operations (see column 3 lines 30-33, "instruction cycle"); said programming tool ("program controlling microcomputer 1"), after said step of editing ("modify") is completed and while said CPU unit ("CPU module 15") is carrying out said cyclic operations ("instruction cycle"), downloads the edited user program ("stored updated user program") to the selected memory ("user program memories 5a, 5b") to be stored; and said CPU unit ("CPU module 15"), after said edited user program is stored ("stored updated user program"), switches ("memory selecting register 6") the object of execution ("executed") from the other memory ("user program

memories 5a, 5b") to the selected memory ("user program memories 5a, 5b") and executes the newly ("new execution") edited user program ("updated user program").

As per claim 9, the Itoh et al. reference discloses a method of processing with a programmable controller by using a programming tool, said programmable controller having two memories for storing a user program and adapted to carry out cyclic operations of I/O refresh, user program execution and peripheral service processes; said method comprising the steps of: preliminarily having said two memories to store user programs with same contents; selecting (see column 2 lines 57-60; "memory selecting register 6") the user program ("user program") stored in a selected one of said two memories (see column 2 line 47, "two user program memories 5a, 5b") as the object of execution (see column 2 lines 44-45, "program executing microcomputer 3") and arranging such that said programming tool (see column 4 lines 14-22, "program controlling microcomputer 1") can write only (see column 4 lines 4-10, "set point 3") into the other of said memories (user program memories 5a, 5b"); transmitting ("read out from") to said programming tool ("program controlling microcomputer 1") the user program (see column 3 lines 52-56, "read out the user program") stored in either of said two memories ("user

program memories 5a, 5b") while said programmable controller (see column 2 line 40, "programmable controller") is carrying out said peripheral service processes (see column 2 line 46, "PI/O bus controller 7") in said cyclic operations (see column 3 lines 30-33, "instruction cycle"); storing the user program (see column 4 lines 16-18, "store the updated user program") from said programming tool ("program controlling microcomputer 1") in said the other of said two memories ("user program memories 5a, 5b") while said programmable controller ("programmable controller") is carrying out said peripheral service processes ("PI/O bus controller 7") in said cyclic operations ("instruction cycle"); switching ("memory selecting register 6") the object of execution (see column 4 lines 30-32, "new execution") from said one of said memories ("user program memories 5a, 5b") to said the other of said memories ("user program memories 5a, 5b") and causing the user program ("user program") stored in said other of said memories ("user program memories 5a, 5b") to be executed; and storing the user program stored in said the other of said memories in said one of said memories and causing the user programs in said two memories to have same contents.

The Itoh et al. reference does not expressly disclose preliminarily having said two memories to store user programs with same contents and storing the user

program stored in said the other of said memories in said one of said memories and causing the user programs in said two memories to have same contents.

The Wilburn reference discloses

(see column 3 lines 41-45, "... allow modification or editing of a program memory ... continuously and interactively controlled by a microprocessor 31 with which the program memory is associated.")

(see column 4 lines 6-12, "... a first program memory 41 ... a second program memory 43 which is essentially similar to the first program memory 41.")

(see column 4 lines 46-48, "The editor 67 ... implement changes in a program memory ...")

(see column 5 lines 39-43, "The editing or patching process ... introduce any desired changes into the algorithms in the program memory being edited without affecting the executing program memory.")

(see column 6 lines 10-14, "... the executing program memory is replaced by with the edited program memory without interrupting operative control of the microprocessor 31")

(see column 6 lines 24-34, "... the algorithms in the first and second program memories will, at some initial time , be identical")

(see column 6 lines 45-60, "... the former executing memory will be placed in the edit mode and the edited memory will become the executing memory ... such interchange of the memories can be accomplished without interruption of the interactive control provided by the microprocessor 31 ... the same editorial changes can be introduced into the formerly executing program.")

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the user program memories taught by the Itoh et al. reference to include identical user programs initially and finally as taught by the Wilburn reference.

One of ordinary skill in the art would have been motivated to modify the user program memories to include identical user programs in the user program memories initially and finally to provide a programmable controller which is capable of editing, verifying, and replacing a user program easily and quickly.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references are cited to further show the state of the art with respect to editing programmable controllers in general:

USPN 5,321,603 to Schwenke

USPN 4,755,997 to Takahashi

JPPN 5-80813 A to OSHIGA et al.

JPPN 59-142792 A to SUZUKI et al.

WO 82/04136 to KIYA

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Crystal J. Barnes whose telephone number is 571.272.3679. The examiner can normally be reached on Monday-Friday alternate Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on 571.272.3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Crystal J Barnes
CJB
21 October 2005